IN THE CLAIMS:

1. (Currently Amended) A liquid crystal display which comprises a pair of substrates and a liquid crystal layer sandwiched between the pair of substrates;

wherein where the alignment state of a liquid crystal when no voltage is applied to the liquid crystal layer is defined as an alignment state 1 and the alignment state of the liquid crystal used for performing displaying is defined as an alignment state 2, the alignment state 1 differs from the alignment state 2;

wherein the alignment state 1 is a splay alignment state whereas the alignment state 2 is a bend alignment state;

wherein source wiring electrodes, gate wiring electrodes, and switching elements are disposed on one of the substrates;

wherein a flattening film is stacked on the switching elements;

wherein pixel electrodes electrically connected to the switching elements are disposed on the flattening film; and

wherein in plan view, the pixel electrodes overlap with the source wiring electrodes or the gate wiring electrodes.

2. (Previously Presented) A liquid crystal display according to claim 1, wherein in plan view, the pixel electrodes overlap with the source wiring electrodes and the gate wiring electrodes.

3. (Previously Presented) A liquid crystal display according to claim 1, wherein the flattening film is composed of a resin layer.

4. and 5. (Canceled)

6. Previously Presented) A liquid crystal display according to claim 1, wherein irregularities are provided on the flattening film, and the level differences of the irregularities are 1 μm or less.

7. (Previously Presented) A liquid crystal display according to claim 6, wherein the level differences of the irregularities are 0.5 μm or less.

8. (Previously Presented) A liquid crystal display according to claim 1, wherein the spacing between the pixel electrodes is within the range of from 1 μm to 10 μm.

9. (Previously Presented) A liquid crystal display according to claim 1, wherein one of the substrates has a plurality of pixel electrodes and the spacing between the pixel electrodes is within the range of from 1 μm to 5 μm.

10. (Currently Amended) A liquid crystal display ~~according to claim 8,~~ which comprises a pair of substrates and a liquid crystal layer sandwiched between the pair of substrates;

wherein where the alignment state of a liquid crystal when no voltage is applied to the liquid crystal layer is defined as an alignment state 1 and the alignment state of the liquid crystal used for performing displaying is defined as an alignment state 2, the alignment state 1 differs from the alignment state 2;

wherein source wiring electrodes, gate wiring electrodes, and switching elements are disposed on one of the substrates;

wherein a flattening film is stacked on the switching elements;

wherein pixel electrodes electrically connected to the switching elements are disposed on the flattening film;

wherein in plan view, the pixel electrodes overlap with the source wiring electrodes or the gate wiring electrodes;

wherein the spacing between the pixel electrodes is within the range of from 1 μm to 10 μm; and

wherein at least part of the pixel electrodes is higher than the average height of the pixel electrodes.

11. (Currently Amended) A liquid crystal display ~~constructed according to Claim 8,~~ which comprises a pair of substrates and a liquid crystal layer sandwiched between the pair of substrates;

wherein where the alignment state of a liquid crystal when no voltage is applied to the liquid crystal layer is defined as an alignment state 1 and the alignment state of the liquid crystal used for performing displaying is defined as an alignment state 2, the alignment state 1 differs from the alignment state 2;

wherein source wiring electrodes, gate wiring electrodes, and switching elements are disposed on one of the substrates;

wherein a flattening film is stacked on the switching elements;

wherein pixel electrodes electrically connected to the switching elements are disposed on the flattening film;

wherein in plan view, the pixel electrodes overlap with the source wiring electrodes or the gate wiring electrodes;

wherein the spacing between the pixel electrodes is within the range of from 1 μm to 10 μm; and

wherein a voltage is applied across the pixel electrodes and an opposed electrode formed on the other one of the pair of substrates, thereby transiting the alignment state of the liquid crystal layer to a bend alignment to perform displaying in the condition after the transition.

12. to 49. (Canceled)